

# Scaling Theory for Conical Surrounding-Gate MOSFET

Durlav Sonowal<sup>1</sup>, Santanu Sarma<sup>2</sup>, Riku Chutia<sup>1</sup>

Assistant Professor, Dept. of ECE, Tezpur University, Sonitpur, India<sup>1</sup> Associate Professor, Dept. of ECE, Tezpur University, Sonitpur, India<sup>2</sup>

**Abstract**: In this paper, we present scaling theory for conical Surrounding-Gate MOSFET which was derived from the cylindrical form of Poisson's equation assuming parabolic potential profile in the radial direction. For performance estimation, device simulation is done and the data were compared with some existing model of cylindrical as well as Double Gate MOSFET. Subthreshold swing and DIBL effects were simulated for this developed model and was compared with cylindrical and DG structure and found that conical structure gives better immunity to the short channel effect.

Keywords: scaling theory, conical MOSFET, SG MOSFET, cylindrical MOSFET

## I. INTRODUCTION

The primary challenge of VLSI design is the integration of an ever increasing number of devices with high yield and reliability. The short channel effect and poor subthreshold characteristic begin to plague as semiconductor devices are scaled to deep sub-micron region. Several novel device geometries has been introduced which has the benefits of both reducing the SCE and improving subthreshold slope as well as potentially higher packing density. Cylindrical structure gives 30% reduction in the natural length over the double gate devices at given  $t_{si}$  and  $t_{ox}$  [1]-[8]. This improvement is due to the stronger influence of the gate over the channel potential in the cylindrical structure. In this paper we have modelled a conical MOSFET and developed the scaling theory for the same. The paper is organized as follows: Section I gives the introduction, Section II presents the proposed conical structure and derivation of the natural length. Section III presents the results showing suthreshold swing and DBIL (Drain Induced Barrier Lowering) effect for double gate, cylindrical, and conical structure.

## II. DERIVATION OF NATURAL LENGTH FOR CONICAL MOSFET



Fig 1. Proposed Conical MOSFET

Poisson's equation for potential,  $\phi(\mathbf{r}, \mathbf{z})$ in cylindrical coordinates is [1],

$$\frac{1}{r}\frac{\partial}{\partial r}r\left(r\frac{\partial}{\partial r}\phi(r,z)\right) + \frac{\partial}{\partial z^2}\phi(r,z) = \frac{qN_a}{\varepsilon_{si}}$$
(1)

www.ijareeie.com



where  $N_a$  is the channel doping (assumed to be uniform). The Poisson's equation can be solved for  $\phi(\mathbf{r}, \mathbf{z})$  such that

$$\phi(r,z) = \phi_c(z) - \left(\frac{2\varepsilon_{si}r^2(\phi_c(z) - \phi_{gs})}{\varepsilon_{si}t_{si}^2\ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + \frac{\varepsilon_{ox}t_{si}^2}{2}}\right)$$
(2)

The above equation is valid for cylindrical structure and gives the potential distribution in a cylindrical MOSFET. At the centre of the pillar, it can be shown that [1],[5]

$$\frac{\partial}{\partial z^2} \phi_c(z) - \frac{(\phi_c(z) - \phi_{gs})}{\lambda_3^2} = \frac{q N_a}{\varepsilon_{si}}$$
(3)

where,  $\lambda_3$  is the natural length for cylindrical MOSFET and is given by,

$$\lambda_3 = \sqrt{\frac{2\varepsilon_{si}t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + \varepsilon_{ox}t_{si}^2}{16\varepsilon_{ox}}} \qquad (4)$$

In our model we divide the conical MOSFET structure into *n* number of cylindrical slices such that the uppermost cylinder has  $t_{si} = t_{si max}$ , and lowermost cylinder has  $t_{si} = t_{si min}$ . Also  $L_{eff}$  for each cylinder is  $L_{eff}/n$ . Here we approximated the natural length  $\lambda_4$  for conical MOSFET by averaging the natural lengths of the uppermost and lowermost cylinders as derived for cylindrical structure.



Fig. 2 Conical MOSFET divided into n number of cylindrical slices

Thus we have 
$$\lambda_4 = \frac{\lambda_{41} + \lambda_{4n}}{2}$$
 (5)  
where  $\lambda_{41} = \sqrt{\frac{2\varepsilon_{si}t_{si\ min}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si\ min}}\right) + \varepsilon_{ox}t_{si\ min}^2}{16\varepsilon_{ox}}}$  (6)

$$\lambda_{4n} = \sqrt{\frac{2\varepsilon_{si}t_{si\,max}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si\,max}}\right) + \varepsilon_{ox}t_{si\,max}^2}{16\varepsilon_{ox}}} \quad (7)$$

Here  $\frac{t_{si max} + t_{si min}}{2} = t_{si}$ ,  $t_{si}$  is the silicon thickness for the cylindrical structure.



Similar to cylindrical and double gate structure we have scaling parameter for conical MOSFET as,  $\alpha_4 = \frac{L_{eff}}{2\lambda_4}$  (8)

Also  $\lambda_4$  has the same physical significance as  $\lambda_1$ ,  $\lambda_2$  and  $\lambda_3$ , the natural length for conventional planner, DG and cylindrical MOSFET respectively.

The scaling parameter  $\alpha$  can be related with the subthreshold swing by the equation [1],

$$s = \frac{\frac{kT}{q}}{\log e} \left[ 1 + \frac{P+Q}{\sqrt{PQ}} e^{-\alpha} \right]^{-1} \quad (9)$$

The Drain Induced Barrier Lowering (DIBL) effect can be approximated with  $\alpha$  as follows [2],

$$DBIL \approx (1 + r_{eff}) \frac{\varepsilon_{si} t_{ox} t_{si}}{\varepsilon_{ox} L_{\rho o}^2}$$
(10)

where Lpo < Lg is the pinched-off channel length [2]-[3], and

$$r_{eff} = -\frac{dV_1}{dV_{GbS}} \quad (11)$$

The subthreshold swing can related with  $r_{eff}$  can be related as

$$S \approx \left(1 + r_{eff}\right) \frac{kT}{q} \ln 10 \quad (12)$$

Thus from equations 9, 10, 11 and 12 we can write

$$DIBL \approx \frac{\log e}{\ln 10} \left[ 1 - \frac{P+Q}{\sqrt{PQ}} e^{-\alpha} \right] \frac{\varepsilon_{si} t_{ox} t_{si}}{\varepsilon_{ox} L_{\rho o}^2}$$
(13)

#### III. RESULTS AND DISCUSSION

The subthreshold swing for double gate, cylindrical, and conical structure are shown in Fig. 3. The Conical device has lowest subthreshold swing that results in least leakage current followed by cylindrical and planar structures.



Fig. 3 Subthreshold swing for planer, cylindrical and conical MOSFET

www.ijareeie.com



The DIBL with respect to effective channel length for planer, cylindrical and conical MOSFETs are shown in Fig. 4. It has been observed that DIBL effect is lowest in a conical structure, followed by cylindrical and planar. From this figure it appears that conical device will have lesser leakage current and also lesser will be the effect of drain voltage on the threshold voltage.



Fig. 4 DIBL effect for planer, cylindrical and conical MOSFET

### REFERENCES

- Cbristopher, I P. A. and Plummer, J. D., "Scaling Theory for Cylindrical, Fully Depleted Surrounding Gate MOSFET", IEEE Electron Device Letters, Vol 18, No.2, February 1997.
- [2] Taur, Y. and Ning, T. H., Fundamentals of Modem VLSI Devices. Cambridge, UK.: Cambridge Univ. Press, 1998.
- [3] Zhicbao, L. and Fossum, J. G., "Short-Channel Effects in Independent-Gate FinFETs ", IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO.2, FEBRUARY 2007
- [4] Yan, R. H., Ourmazrl, A. and Lee, K. F., "Scaling the Si MOSFET: From Bulk to SOI to Bulk", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 39, No.7, JULY 1992.
- [5] Chiang, T.K., "A New Scaling Theory for fully-depleted SOI Double-Gate MOSFET's: including effective conducting path effect (ECPE)", Elsevier Science: Microelectronic Engineering, Vol 77 Issue 2, February 2005.
- [6] Martino, J. A. and Pavanello, M. A., "DmL Evaluation for 0.13 ~m Floating-Body Partially Depleted SOI MOSFET in Low Temperature Operation", The Electrochemical Society, Inc, Abs. 876, 204th Meeting, 2003.
- [7] Kumar, M. J., Orouji, Ali A., and Dbakad, H., "New Dual-Material SG Nanoscale MOSFET: Analytical Threshold-Voltage Model", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO.4, APRIL 2006.
- [8] Oh S. H., Monroe, D. and Hergenrother, O. M., "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs", IEEE ELECTRON DEVICE LETTERS, VOL. 21, NO.9, SEPTEMBER 2000.